Applicant respectfully requests reconsideration of claims 22-34 in view of the foregoing amendments and the following remarks. Some of the technical differences between the applied references and embodiments of the invention will now be discussed. Of course, these discussed differences regarding the embodiments, which are disclosed in detail in the patent specification, do not define the scope or interpretation of any of the claims. Where presented below, such discussed differences merely help the Examiner appreciate important claim distinctions discussed thereafter.

Generally, the disclosed invention is directed to methods and apparatus having trench isolation structures with reduced isolation pad heights and reduced edge spacers. In one embodiment, an apparatus comprises a structure including a semiconductor substrate, a gate oxide layer formed on the substrate, and a first gate layer formed on the gate oxide layer. The structure includes a trench at least partially disposed therein. A field oxide is formed in the trench to a field oxide level that is between an upper surface of the substrate and an upper surface of the first gate layer defining the height of a gate structure. Preferably, the field oxide level is approximately halfway between the surface of the substrate and the height of the gate structure (the first gate layer).

The apparatus having a trench with a field oxide level between the surface of the substrate and the surface of the first gate layer provides a reduced height of the field oxide "isolation pad" compared with prior art trench isolation structures. The reduced isolation pad height advantageously reduces or eliminates an edge spacer that may otherwise form along the edges of the isolation pad during the process of forming an edge spacer on the gate structure adjacent to the isolation pad. Therefore, the isolation structures require less area on the apparatus.

I. Claim Amendments and New Claims.

Applicants have amended claims 22 and 23 to better point out and distinctly claim the subject matter which Applicants regard as their invention. Specifically, Applicants have amended claim 22 to reflect that the first gate layer may be formed from materials other than polysilicon, and to more specifically recite the existence of the trench. Claim 23 has been amended to depend from claim 22. Claims 35-37 have been added. No new matter has been added.

II. Rejection of claims 22, 32, and 34 under 35 USC § 102(b) as being anticipated by Manning (US 5,177,028).

The Examiner rejected claims 22, 32, and 34 under 35 USC § 102(b) as being anticipated by Manning (US 5,177,028).

Manning teaches trench isolation methods including (1) forming a pad oxide layer on the substrate (4:8-10), (2) forming a first polysilicon layer on the pad oxide layer (4:18-19), (3) etching the first polysilicon layer, pad oxide layer, and substrate to form isolation trenches and mesa areas (4:39-48), (4) lightly oxidizing the isolation trenches to repair damage thereto (4:49-52), (5) forming an isolation oxide layer within the isolation trenches "to a thickness which is sufficient to fill isolation trenches 108" (4:54-55), (6) removing the isolation oxide layer above the mesa areas (4:56-57) "until all oxide 112 is removed over mesa areas 110, leaving isolation trenches 108 filled with oxide 112" (5:3-5), and (7) forming a second polysilicon layer over the first polysilicon layer (5:16-19). Thus, according to the teachings of Manning, the resulting microelectronics structure includes a first polysilicon layer, an isolation oxide layer that fills the isolation trench, and a second polysilicon layer. Furthermore, according to Manning, the first polysilicon layer is sufficiently thin "to enable FET gate threshold implanting therethrough" (4:31), and the second polysilicon layer "is conductively doped, since it will form the FET gates" (5:19-20).

Alternately, Manning teaches forming etch stop layers on the first polysilicon layer prior to etching the isolations trenches. According to the teachings of Manning, the first polysilicon layer gives added height to the isolation oxide layer extending from the trenches, "thus decreasing the likelihood of forming parasitic transistors on trench sidewalls by removing too much oxide." (6:20-24). One of the claimed advantages of the methods taught by Manning is that "the thin first layer of polysilicon adds height to the trench oxide" (6:35-37).

On the other hand, Applicants claim 22 (as amended) recites microelectronics devices including a microelectronic substrate, a structure including a gate oxide layer formed on the substrate and a first gate layer formed on the gate oxide layer, the structure having a trench at least partially disposed therein and extending into the substrate, and a field oxide layer at least partially in the trench, the field oxide layer having a field oxide level between the level of an upper surface of the substrate

and the level of an upper surface of the first gate layer. The first gate layer may be a polysilicon layer (5:24-26).

Manning does not anticipate apparatus as recited in Applicants' claims 22 because according to Manning, the isolation oxide layer within the isolation trenches is filled "to a thickness which is sufficient to fill isolation trenches 108" (4:54-55), after which "all oxide 112 is removed over mesa areas 110, leaving isolation trenches 108 filled with oxide 112" (5:3-5). Manning does not disclose, teach or suggest "the field oxide layer having a field oxide level between the level of an upper surface of the substrate and the level of an upper surface of the first gate layer" as recited in Applicants' claim 22.

Similarly, Applicants' claim 32 recites a microelectronic device comprising a microelectronic substrate having a trench formed in a surface thereof, a gate structure formed on the substrate, and a field oxide deposited in the trench, the field oxide extending from the trench beyond the surface of the substrate by a height which is less than or equal to approximately one half of a height of the gate structure formed on the substrate. Manning does not anticipate apparatus as recited in Applicants' claims 32 because according to Manning, the isolation oxide layer within the isolation trenches is filled "to a thickness which is sufficient to fill isolation trenches 108" (4:54-55), after which "all oxide 112 is removed over mesa areas 110, leaving isolation trenches 108 filled with oxide 112" (5:3-5). Thus, according to Manning, the field oxide extends at least to the height of the first polysilicon layer to give added height to the isolation oxide layer extending from the trenches (6:20-24). One of the claimed advantages of the methods taught by Manning is that "the thin first layer of polysilicon adds height to the trench oxide" (6:35-37). Manning does not disclose, teach or suggest "the field oxide extending from the trench beyond the surface of the substrate by a height which is less than or equal to approximately one half of a height of the gate structure formed on the substrate" as recited in Applications claim 32.

Furthermore, Applicants' claim 34 recites a microelectronic device comprising a microelectronic substrate having a trench formed therein, and a field oxide within the trench and projecting therefrom by a height which is small enough to prevent the formation of spacers adjacent the field oxide pad. Manning does not anticipate claim 34 because, according to Manning, the field oxide fills the isolation trenches to at least the level of the first polysilicon layer, and in alternate

embodiments, teaches using the first polysilicon layer to give added height to the isolation oxide layer extending from the trenches (6:20-24). One of the claimed advantages of the methods taught by Manning is that "the thin first layer of polysilicon adds height to the trench oxide" (6:35-37). Manning does not disclose, teach or suggest "a field oxide within the trench and projecting therefrom by a height which is small enough to prevent the formation of spacers adjacent the field oxide pad" as recited in Applications claim 34.

Dependent claims 23-25, 33, and 35-37 are also not anticipated by Manning, for the reasons cited above, and for other limitations which further distinguish over Manning. For example, claim 23 recites a polysilicon adhesion layer formed on the first gate layer. Claims 24 and 25 further recite silicide and tungsten silicide layers, respectively, formed on the polysilicon adhesion layer. Claim 33 recites an oxide spacer adjacent the gate structure. Claim 36 specifies that the field oxide level is approximately one half the distance between the upper surface of the substrate and the upper surface of the first gate layer. Claim 37, which depends from claim 24, further specifies that the field oxide level is less than or equal to approximately one half the distance between the upper surface of the substrate and the upper surface of the silicide layer.

For the foregoing reasons, Applicants submit that claims 22, 32, and 34 are not anticipated by Manning, and respectfully request the reconsideration and withdrawn of this rejection.

III. Rejection of claims 23-25 and 33 under 35 USC § 103(a) as being unpatentable over Applicant's Admitted Prior Art Figure 1 in view of Manning (US 5,177,028).

The Examiner rejected claims 23-25 and 33 under 35 USC § 103(a) as being unpatentable over Applicant's Admitted Prior Art Figure 1 in view of Manning (US 5,177,028).

As noted on page 3 of Applicant's specification, Prior Art Figure 1 shows a conventional shallow trench isolation structure 10 fabricated on a microelectronic substrate 20. Gate structures 100 and 300 are formed on the substrate 20 from a pad/gate oxide layer 30, a first gate layer 40, a second gate layer 70 and a silicide layer 80. A trench 22 formed in the substrate 20 is filled with a silicon oxide 60, to form the shallow trench isolation structure or isolation pad 400. An isolated component 200 is fabricated on the isolation pad 400, the isolated component 200

comprising the second gate layer 70 and the silicide layer 80. Oxide spacers 91 - 94 are then formed about the gate structures 100 and 300, the isolated component 200 and the isolation pad 400. The oxide spacers 91-94 protect the components from contact with other conductive components, as well as, providing gentle slopes to improve step coverage when applying additional layers. Generally, the less severe the slope, the better the coverage. As shown in Prior Art Figure 1 and described on page 3 of Applicant's specification, the spacers 91-94 take up a large amount of area on the microelectronic substrate 20.

The teachings of Manning were discussed in the preceding section and, for the sake of brevity, are incorporated herein by reference. Importantly, Manning teaches that the first polysilicon layer gives added height to the isolation oxide layer extending from the trenches, "thus decreasing the likelihood of forming parasitic transistors on trench sidewalls by removing too much oxide." (6:20-24). One of the claimed advantages of the methods taught by Manning is that "the thin first layer of polysilicon adds height to the trench oxide" (6:35-37). As shown in Manning's Figure 18, the isolation oxide layer 112a actually extends above the first polysilicon layer 106a, or at least fills the isolation trenches 108. (5:4-5).

The combination of Prior Art Figure 1 and Manning does not teach or suggest apparatus as claimed by Applicants. Prior Art Figure 1 shows isolation oxide layers which extend above the substrate to a height equal to the height of the upper surface of the first gate layer. Manning teaches not only that the isolation oxide layers should extend above the surface of the substrate to the upper surface of the first polysilicon layer (*i.e.* fills the isolation trenches 108, 5:4-5), but further teaches that the first polysilicon layer may be used in combination with an etch stop layer to extend the height of the isolation oxide layer even further above the substrate (Figure 18, 6:20-24). Manning clearly suggests that increasing the height of the isolation oxide layer is desirable and advantageous (6:35-37).

Because Manning strongly teaches that *increasing* the height of the isolation oxide layer above the substrate is advantageous in order to reduce the formation of parasitic transistors on trench sidewalls, Manning teaches away from Applicants' claimed apparatus. On the other hand, Applicants teach that it is desirable to *reduce* the height of the isolation oxide layer in comparison with Prior Art Figure 1. Therefore, Manning clearly teaches away from the apparatus according to Applicants' invention.

Claim 23 (as amended) depends from claim 22. Applicants claim 22 recites microelectronics devices including a microelectronic substrate, a structure including a gate oxide layer formed on the substrate and a first gate layer formed on the gate oxide layer, the structure having a trench at least partially disposed therein and extending into the substrate, and a field oxide layer at least partially in the trench, the field oxide layer having a field oxide level between the level of an upper surface of the substrate and the level of an upper surface of the first gate layer. Neither Prior Art Figure 1 nor Manning, nor the combination of Prior Art Figure 1 and Manning, disclose, teach or suggest a device having a field oxide level between the level of an upper surface of the substrate and the level of an upper surface of the first gate layer. Particularly, neither reference nor the combination of references teaches a device wherein the field oxide level is less than or equal to approximately one half the distance between the upper surface of the substrate and the upper surface of the first gate layer, as recited in claim 36.

Similar distinguishing limitations are found in Applicants' independent claims 26, 28, 30, and 32. With respect to claim 33 which was rejected by the Examiner over the combination of Prior Art Figure 1 and Manning, claim 33 depends from claim 32. Claim 32 recites a microelectronic device comprising a microelectronic substrate having a trench formed in a surface thereof, a gate structure formed on the substrate, and a field oxide deposited in the trench, *the field oxide extending from the trench beyond the surface of the substrate by a height which is less than or equal to approximately one half of a height of the gate structure formed on the substrate.* (emphasis added). Again, neither Prior Art Figure 1 nor Manning, either singly or in combination, discloses having a field oxide level proportionate to a gate structure height as recited in claim 32.

Furthermore, claim 34 recites a microelectronic device comprising a microelectronic substrate having a trench formed therein, and *a field oxide within the trench and projecting therefrom by a height which is small enough to prevent the formation of spacers adjacent the field oxide pad.* Neither Prior Art Figure 1 nor Manning, either singly or in combination, discloses having a field oxide level small enough to prevent the formation of spacers as recited in claim 34.

Dependent claims 23-25, 33, and 35-37 are also not obvious over the combination of Prior Art Figure 1 and Manning, for the reasons cited above, and for other limitations contained therein. For example, claim 23 recites a polysilicon

adhesion layer formed on the first gate layer. Claims 24 and 25 further recite silicide and tungsten silicide layers, respectively, formed on the polysilicon adhesion layer. Claim 33 recites an oxide spacer adjacent the gate structure. Claim 36 specifies that the field oxide level is approximately one half the distance between the upper surface of the substrate and the upper surface of the first gate layer. Claim 37, which depends from claim 24, further specifies that the field oxide level is less than or equal to approximately one half the distance between the upper surface of the substrate and the upper surface of the silicide layer. These limitations, together with the limitations of the base claims, are not disclosed or suggested by the combination of Prior Art Figure 1 and Manning.

For the foregoing reasons, Applicants submit that claims 23-25 and 33 are not are not obvious over the combination of Prior Art Figure 1 and Manning, and respectfully request the reconsideration and withdrawn of this rejection.

IV. Rejection of claims 26-31 under 35 USC § 112, first paragraph, as containing subject matter that was not described in the specification.

The Examiner rejected claims 26-31 under 35 USC § 112, first paragraph, as containing subject matter that was not described in the specification.

Applicants have amended the specification at page 7, lines 20-22, to recite (as amended) that "the field oxide isolation pad height 66 may be a height between the height of the first gate layer and the surface of the substrate. Preferably, the isolation pad height 66 may be less than or equal to approximately one half of the height of the gate structure 106, 306, or the height of the isolated component 200 (Figure 2H), or for embodiments having only the first gate layer 40 (Figure 2E), less than or equal to approximately one half of the height of the first gate layer 40 (*i.e.* less than or equal to an approximately two-to-one ratio). Even more preferably, the field oxide isolation pad height 66 may be small enough to completely prevent the formation of spacers adjacent the field oxide isolation pad." These amendments find support in the original disclosure, including specification page 6, lines 21 through 28, and claims 2-5, 11, 19, 22, 23, 26, 28, 30, 32, and 34. No new matter has been added.

Applicants submit that the specification as amended contains a description of the subject matter is such a way as to reasonably convey to one skilled in the relevant art that the inventors had possession of the claims invention at the time

the application was filed. Applicants respectfully ask the Examiner to reconsider and withdraw the rejection of claims 26-31.

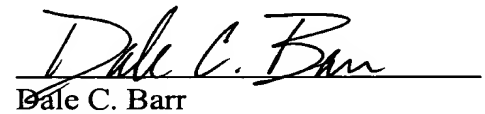
Conclusion

In light of the foregoing amendments and remarks, Applicant believes that claims 22-37 are in condition for allowance, and that action is respectfully requested.

The Assistant Commissioner is authorized to charge payment of any fees under 37 C.F.R. §§ 1.16 and 1.17 associated with this communication or credit any overpayment to Deposit Account No. 50-1266.

If there are any remaining matters that can be handled in a telephone conference, Applicant invites the Examiner to phone his attorney, Dale C. Barr, at (206) 903-8745.

Respectfully submitted,
DORSEY & WHITNEY LLP



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